

AMENDMENTS

Listing of Claims

This listing of claims replaces all prior versions and listings of claims in the application.

- 1 1. (Currently amended) A system for generating amplitude matched,
2 phase shifted signals, comprising:
3 a filter arrangement including a plurality of input and output nodes, a first set of
4 input nodes arranged to receive an input signal, a second set of input nodes coupled to
5 electrical ground, each output node configured to provide an associated vector that is
6 offset in phase from a vector associated with each other output node; and
7 an adjustable element associated with each output node, the adjustable element
8 configured to receive a feedback signal and in response to the feedback signal
9 substantially equalize an amplitude of each vector associated with each output node.

- 1 2. (Currently amended) The system of claim 1, wherein four output
2 nodes are associated with the filter arrangement, each output node having an associated
3 vector.

- 1 3. (Original) The system of claim 2, further comprising:
2 an adder element configured to add the four vectors resulting in eight phase
3 shifted vectors.

- 1 4. (Original) The system of claim 3, further comprising:
2 a scaler configured to scale the amplitude of the four vectors resulting in eight
3 amplitude matched phase shifted vectors.

- 1 5. (Original) The system of claim 4, wherein the adjustable element is
2 an adjustable resistance.

1 6. (Original) The system of claim 5, wherein the adjustable resistance
2 is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

1 7. (Original) The system of claim 4, wherein the adjustable element is
2 an adjustable capacitance.

1 8. (Original) The system of claim 7, wherein the adjustable
2 capacitance is a varactor.

1 9. (Currently amended) A method for generating amplitude matched,
2 phase shifted signals, comprising:
3 providing a plurality of vectors, each vector associated with a respective output
4 node, each vector offset in phase from each other vector associated with each other
5 output node;
6 applying an input signal at a subset of a set of input nodes;
7 providing a feedback signal to a respective adjustable element associated with
8 each input and output node; and
9 adjusting each ~~node~~ adjustable element using the feedback signal to
10 substantially equalize an amplitude of each vector associated with each output node.

1 10. (Currently amended) The method of claim 9, wherein a resistance
2 associated with each output node is adjusted to substantially equalize an amplitude of
3 each vector associated with each output node.

1 11. (Currently amended) The method of claim 9, wherein a capacitance
2 associated with each output node is adjusted to substantially equalize an amplitude of
3 each vector associated with each output node.

1 12. (Original) The method of claim 10, further comprising adjusting the
2 resistance using a metal oxide semiconductor field effect transistor (MOSFET)
3 adjustable resistance.

1 13. (Currently amended) The method of claim 12, further comprising
2 combining four vectors associated with each of four output nodes resulting in eight
3 phase shifted vectors.

1 14. (Original) The method of claim 13, further comprising scaling the
2 four vectors resulting in eight substantially amplitude matched phase shifted vectors.

1 15. (Original) The method of claim 11, further comprising adjusting the
2 capacitance using a varactor.

1 16. (Currently amended) The method of claim 15, further comprising
2 combining four vectors associated with each of four output nodes resulting in eight
3 phase shifted vectors.

1 17. (Original) The method of claim 16, further comprising scaling the
2 four vectors resulting in eight amplitude matched phase shifted vectors.

1 18. (Currently amended) A system for generating amplitude matched,
2 phase shifted signals, comprising:
3 filter means including a plurality of input and output nodes, a first set of input
4 nodes arranged to receive an input signal, a second set of input nodes coupled to
5 electrical ground, the filter means for providing a plurality of associated vectors that are
6 offset in phase from each other vector associated with each other output node;
7 means for providing a feedback signal to an adjustable element associated with
8 each output node; and
9 means for using the feedback signal to substantially equalize an amplitude of
10 each vector associated with each output node.

1 19. (Original) The system of claim 18, wherein the means for
2 substantially equalizing an amplitude of each vector comprises adjustable resistance
3 means.

1 20. (Original) The system of claim 18, wherein the means for
2 substantially equalizing an amplitude of each vector comprises adjustable capacitance
3 means.

1 21. (Original) The system of claim 19, wherein the adjustable resistance
2 means comprises a metal oxide semiconductor field effect transistor (MOSFET)
3 adjustable resistance.

1 22. (Currently amended) The system of claim 21, further comprising:
2 adder means for combining four vectors associated with each of four output
3 nodes resulting in eight phase shifted vectors.

1 23. (Original) The system of claim 22, further comprising:
2 scaler means for scaling an amplitude of the four vectors resulting in eight
3 substantially amplitude matched phase shifted vectors.

1 24. (Currently amended) A system for generating amplitude matched,
2 phase shifted signals, in a portable communication device, comprising:
3 a portable communication device including a transmitter and a receiver;
4 a synthesizer for providing a local oscillator signal;
5 a filter arrangement configured to operate on the local oscillator signal, the filter
6 arrangement including a plurality of input and output nodes, a first set of input nodes
7 arranged to receive the local oscillator signal, a second set of input nodes coupled to
8 electrical ground, each output node configured to provide an associated vector that is
9 offset in phase from a vector associated with each other output node; and
10 an adjustable element associated with each output node, the adjustable element
11 configured to receive a feedback signal and in response to the feedback signal
12 substantially equalize an amplitude of each vector associated with each output node.

1 25. (Currently amended) The system of claim 24, wherein four output
2 nodes are associated with the filter arrangement, each output node having an associated
3 vector.

1 26. (Original) The system of claim 25, further comprising:
2 an adder element configured to add the four vectors resulting in eight phase
3 shifted vectors.

1 27. (Original) The system of claim 26, further comprising:
2 a scaler configured to scale an amplitude of the four vectors resulting in eight
3 substantially amplitude matched phase shifted vectors.

1 28. (Original) The system of claim 27, wherein the adjustable element
2 is an adjustable resistance.

1 29. (Original) The system of claim 28, wherein the adjustable resistance
2 is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

1 30. (Original) The system of claim 27, wherein the adjustable element
2 is an adjustable capacitance.

1 31. (Original) The system of claim 30, wherein the adjustable
2 capacitance is a varactor.